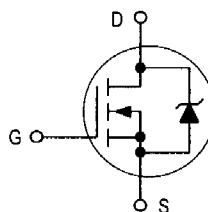


Designer's™ Data Sheet  
**TMOS E-FET™**  
**Power Field Effect Transistor**  
**N-Channel Enhancement-Mode Silicon Gate**

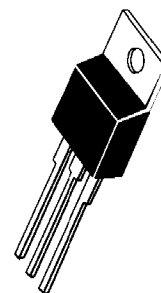
This high voltage MOSFET uses an advanced termination scheme to provide enhanced voltage-blocking capability without degrading performance over time. In addition, this advanced TMOS E-FET is designed to withstand high energy in the avalanche and commutation modes. The new energy efficient design also offers a drain-to-source diode with a fast recovery time. Designed for high voltage, high speed switching applications in power supplies, converters and PWM motor controls, these devices are particularly well suited for bridge circuits where diode speed and commutating safe operating areas are critical and offer additional safety margin against unexpected voltage transients.

- Robust High Voltage Termination
- Avalanche Energy Specified
- Source-to-Drain Diode Recovery Time Comparable to a Discrete Fast Recovery Diode
- Diode is Characterized for Use in Bridge Circuits
- $I_{DSS}$  and  $V_{DS(on)}$  Specified at Elevated Temperature



**MTP4N80E**

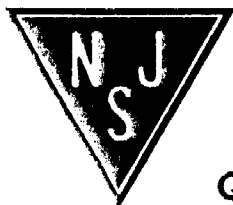
**TMOS POWER FET**  
**4.0 AMPERES**  
**800 VOLTS**  
 $R_{DS(on)} = 3.0 \text{ OHM}$



TO-220AB

**MAXIMUM RATINGS** ( $T_C = 25^\circ\text{C}$  unless otherwise noted)

Rating	Symbol	Value	Unit
Drain-Source Voltage	$V_{DSS}$	800	Vdc
Drain-Gate Voltage ( $R_{GS} = 1.0 \text{ M}\Omega$ )	$V_{DGR}$	800	Vdc
Gate-Source Voltage — Continuous	$V_{GS}$	$\pm 20$	Vdc
— Non-Repetitive ( $t_p \leq 10 \text{ ms}$ )	$V_{GSM}$	$\pm 40$	Vpk
Drain Current — Continuous	$I_D$	4.0	Adc
— Continuous @ $100^\circ\text{C}$	$I_D$	2.9	
— Single Pulse ( $t_p \leq 10 \mu\text{s}$ )	$I_{DM}$	12	Apk
Total Power Dissipation	$P_D$	125	Watts
Derate above $25^\circ\text{C}$		1.0	W/ $^\circ\text{C}$
Operating and Storage Temperature Range	$T_J, T_{stg}$	-55 to 150	$^\circ\text{C}$
Single Pulse Drain-to-Source Avalanche Energy — Starting $T_J = 25^\circ\text{C}$ ( $V_{DD} = 100 \text{ Vdc}$ , $V_{GS} = 10 \text{ Vdc}$ , $I_L = 8.0 \text{ Apk}$ , $L = 10 \text{ mH}$ , $R_G = 25 \Omega$ )	$E_{AS}$	320	mJ
Thermal Resistance — Junction to Case	$R_{\theta JC}$	1.0	$^\circ\text{C/W}$
— Junction to Ambient	$R_{\theta JA}$	62.5	
Maximum Lead Temperature for Soldering Purposes, 1/8" from case for 10 seconds	$T_L$	260	$^\circ\text{C}$



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**Quality Semi-Conductors**

# MTP4N80E

## ELECTRICAL CHARACTERISTICS (T<sub>J</sub> = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
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### OFF CHARACTERISTICS

Drain-Source Breakdown Voltage (V <sub>GS</sub> = 0 Vdc, I <sub>D</sub> = 250 μAdc) Temperature Coefficient (Positive)	V <sub>(BR)DSS</sub>	800 —	— 1.02	— —	Vdc mV/°C
Zero Gate Voltage Drain Current (V <sub>DS</sub> = 800 Vdc, V <sub>GS</sub> = 0 Vdc) (V <sub>DS</sub> = 800 Vdc, V <sub>GS</sub> = 0 Vdc, T <sub>J</sub> = 125°C)	I <sub>DSS</sub>	— —	— —	10 100	μAdc
Gate-Body Leakage Current (V <sub>GS</sub> = ± 20 Vdc, V <sub>DS</sub> = 0)	I <sub>GSS</sub>	—	—	100	nAdc

### ON CHARACTERISTICS (1)

Gate Threshold Voltage (V <sub>DS</sub> = V <sub>GS</sub> , I <sub>D</sub> = 250 μAdc) Temperature Coefficient (Negative)	V <sub>GS(th)</sub>	2.0 —	3.0 7.0	4.0 —	Vdc mV/°C
Static Drain-Source On-Resistance (V <sub>GS</sub> = 10 Vdc, I <sub>D</sub> = 2.0 Adc)	R <sub>DS(on)</sub>	—	1.95	3.0	Ohm
Drain-Source On-Voltage (V <sub>GS</sub> = 10 Vdc) (I <sub>D</sub> = 4.0 Adc) (I <sub>D</sub> = 2.0 Adc, T <sub>J</sub> = 125°C)	V <sub>DS(on)</sub>	— —	8.24 —	12 10	Vdc
Forward Transconductance (V <sub>DS</sub> = 15 Vdc, I <sub>D</sub> = 2.0 Adc)	g <sub>FS</sub>	2.0	4.3	—	mhos

### DYNAMIC CHARACTERISTICS

Input Capacitance	(V <sub>DS</sub> = 25 Vdc, V <sub>GS</sub> = 0 Vdc, f = 1.0 MHz)	C <sub>iss</sub>	—	1320	2030	pF
Output Capacitance		C <sub>oss</sub>	—	187	400	
Reverse Transfer Capacitance		C <sub>rss</sub>	—	72	160	

### SWITCHING CHARACTERISTICS (2)

Turn-On Delay Time	(V <sub>DD</sub> = 400 Vdc, I <sub>D</sub> = 4.0 Adc, V <sub>GS</sub> = 10 Vdc, R <sub>G</sub> = 9.1 Ω)	t <sub>d(on)</sub>	—	13	30	ns
Rise Time		t <sub>r</sub>	—	36	90	
Turn-Off Delay Time		t <sub>d(off)</sub>	—	40	80	
Fall Time		t <sub>f</sub>	—	30	75	
Gate Charge (See Figure 8)	(V <sub>DS</sub> = 400 Vdc, I <sub>D</sub> = 4.0 Adc, V <sub>GS</sub> = 10 Vdc)	Q <sub>T</sub>	—	36	80	nC
		Q <sub>1</sub>	—	7.0	—	
		Q <sub>2</sub>	—	16.5	—	
		Q <sub>3</sub>	—	12	—	

### SOURCE-DRAIN DIODE CHARACTERISTICS

Forward On-Voltage (1)	(I <sub>S</sub> = 4.0 Adc, V <sub>GS</sub> = 0 Vdc) (I <sub>S</sub> = 4.0 Adc, V <sub>GS</sub> = 0 Vdc, T <sub>J</sub> = 125°C)	V <sub>SD</sub>	— —	0.812 0.7	1.5 —	Vdc
Reverse Recovery Time (See Figure 14)	(I <sub>S</sub> = 4.0 Adc, V <sub>GS</sub> = 0 Vdc, dI <sub>S</sub> /dt = 100 A/μs)	t <sub>rr</sub>	—	557	—	ns
		t <sub>a</sub>	—	100	—	
		t <sub>b</sub>	—	457	—	
Reverse Recovery Stored Charge		Q <sub>RR</sub>	—	2.33	—	

### INTERNAL PACKAGE INDUCTANCE

Internal Drain Inductance (Measured from contact screw on tab to center of die) (Measured from the drain lead 0.25" from package to center of die)	L <sub>D</sub>	—	3.5 4.5	—	nH
Internal Source Inductance (Measured from the source lead 0.25" from package to source bond pad)	L <sub>S</sub>	—	7.5	—	nH

(1) Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2%.

(2) Switching characteristics are independent of operating junction temperature.